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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,551	05/13/2004	Yao-Jen Liang	MTKP0118USA	3550

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EXAMINER
VIDWAN, JASJIT S

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,551	LIANG ET AL.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii et al U.S. Patent No: 5,898,695 **[herein after Fujii]** and further in view of Ling et al, U.S. Patent No: 6,732,255 **[herein after Ling]**.

3. **As per Claim 1**, Fujii teaches a method for transmitting data, the system comprising at least a host unit **[see Fig. 5, element 12, "Micro-Processor"]** and at least a slave unit **[see Fig. 5, element 141, "Transfer Buffer"]**, the method comprising the following steps:

> (a) Slave unit informing the host unit of data needs to be transmitted **[Col. 6, Lines 55-60, "a transfer request signal "DREQ" is outputted..."]**
>
> (b) When being informed by the slave unit, the host unit informing the slave unit to start to transmit the data **[Col. 6, Lines 55-60, "...transfer acknowledge signal DACK is sent back"]**
>
> (c) When being informed by the host unit, slave unit starting to transmit the data to the host unit **[Col. 6, Lines 55-60, "...and data is written in RAM without passing through the register of the microprocessor."]**

Fujii does not explicitly teach a method wherein the host unit and slave unit are indefinitely on two different circuit boards (off chip). However, Ling teaches the above limitation wherein buffer memory (slave unit) is off-chip from the microprocessor (host unit) **[see Ling, Col. 7, Lines 1-11]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to have the slave unit and the host unit on different chips because Ling teaches the buffer (slave unit)

working equally well in transmitting data whether the buffer is on-chip or off-chip **[see Ling, Col. 2, Lines 20-26]**.

4. **As per Claim 2**, Fujii as modified by Ling above teaches a method wherein the host chips further delivers a clock signal to the slave chip **[see Fujii, Fig. 5, element 4]**.

5. **As per Claim 3**, Fujii as modified by Ling above teaches wherein the slave chip actively alters a voltage on a request pin pair, electrically connected between the host chip and the slave chip, to inform the host chip of the data needed to be transmitted **[see Fujii, Fig. 5, Element 'DREQ']**

6. **As per Claim 4**, Fujii as modified by Ling above teaches a method wherein the slave chip detects states of a plurality of signals, when any changes of the states of the plurality of the signals are detected, the slave chip actively alters a voltage on a request pin pair to inform the host chip of the data needed to be transmitted, wherein the request pin pair is electrically connected between the host chip and the slave chip **[see Fujii, Col. 9, Lines 61-67]**.

7. **As per Claim 5**, Fujii as modified by Ling above teaches a method wherein the host chip detects a voltage on a request pin pair, when the host chip detects that the voltage on the request pin pair has changed, the host chip delivers a clock signal to the slave chip via a clock pin pair, wherein the request pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip **[see Fujii, Fig. 5, Element 'BUSCLOCK']**

8. **As per Claim 6**, Fujii as modified by Ling above teaches a method wherein the host chip alters a voltage on a latch pin pair for informing the slave chip to start transmitting the data, wherein the latch pin pair is electrically connected between the host chip and the slave chip **[see Fujii, Fig. 5, Element 'DACK']**

1. **As per Claim 7**, Fujii as modified by Ling above teaches a method wherein the slave chip transmits the data to the host chip via a data pin pair on a basis of a clock signal of a clock pin pair, wherein the data pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip **[see Fujii, Col. 6, Lines 49-53]**.

2. **As per Claim 8**, Fujii as modified by Ling above teaches a method wherein the slave chip transmits states of a plurality of signals to the host chip via a data pin pair on a basis of a clock signal of a

clock pin pair, wherein the data pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip **[see Fujii, Col. 4, Lines 44-50]**.

3. **As per Claim 9**, Fujii as modified by Ling above teaches a method wherein the method further comprises the host chip receiving data from the slave chip and decoding the data **[see Fujii, Col. 4, Line 66 – Col. 5, Line 3]**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
8/14/06

August 21, 2006